Determining the Existence of DC Operating Points in Circuits

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Joint work with Ian Mitchell and Mark Greenstreet

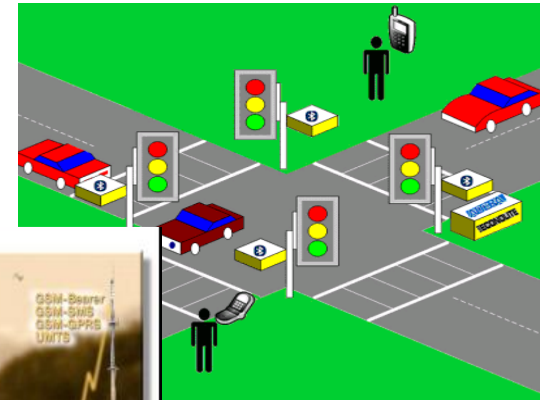
Nov 23rd, 2009

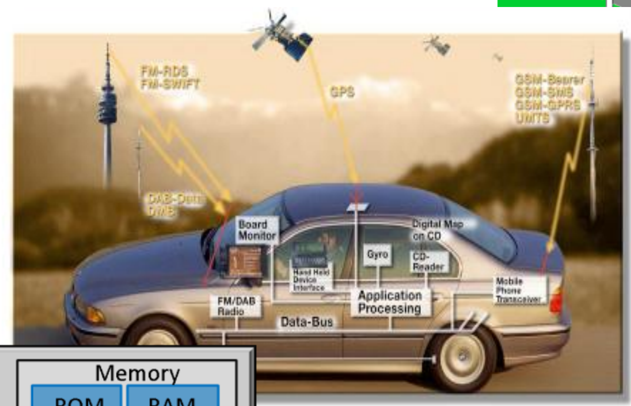
Talk Outline

- Introduction
- Formal Verification of Circuits: An Overview
- DC Analysis:
  - Basic Concepts
  - A Formal Approach
- Case Studies
- Enhancing the Verification with invariants
- Discussion

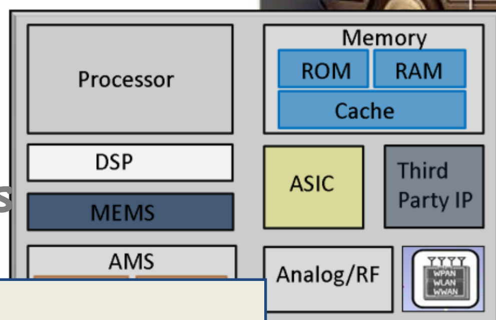
Hybrid Systems

Transportation Systems

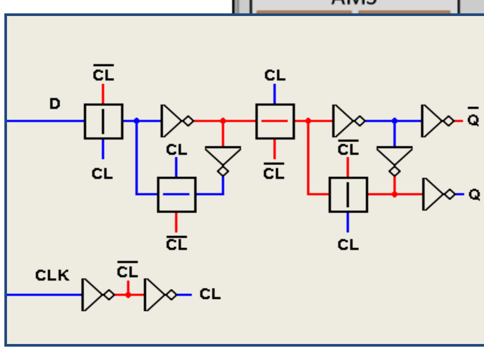




Vehicle:
Mechanical + Computer System



Computer System
Digital and AMS designs

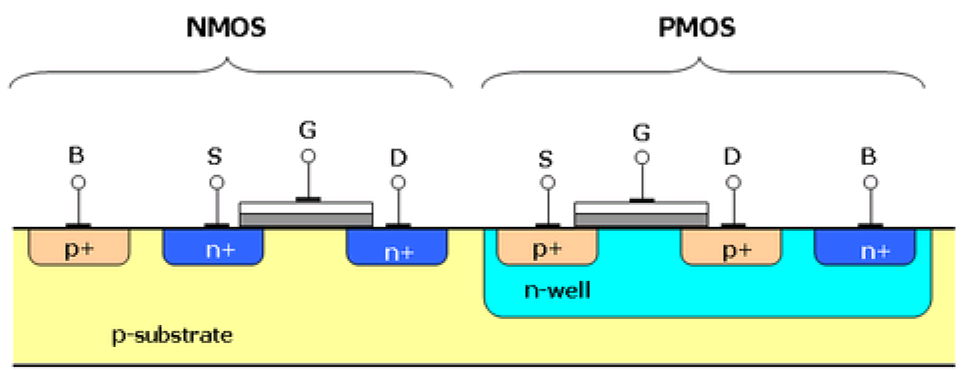


Digital Design

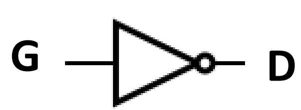
http://www.eecs.berkeley.edu/~apinto/esd
http://www.cs.unc.edu/~templar/
http://nortonkit.net/

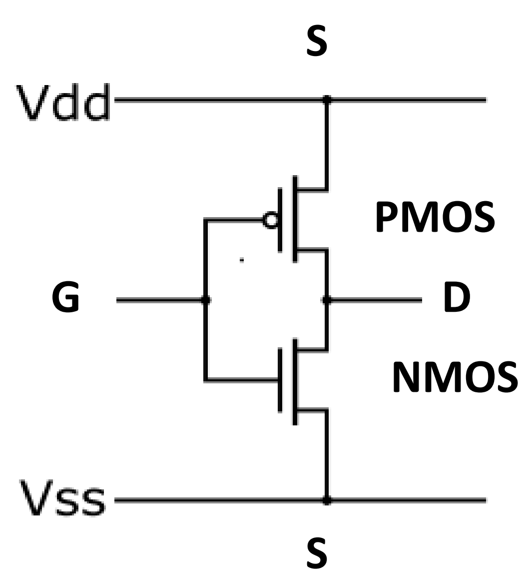
CMOS Design: An introduction

CMOS: **Complementary metal–oxide–semiconductor**
Building blocks of integrated circuits and microprocessors



Example





http://wikipedia.org/

Circuits Verification

- Transistor level models
- Circuit simulator (Spice)
  - Steady State simulation
  - AC simulation
  - Transient simulation
  - Parameter sweeping
  - Statistical variation (Monte Carlo)

Slide based on Kevin Jones talk at FMCAD'09, Portland, USA

DC operating point

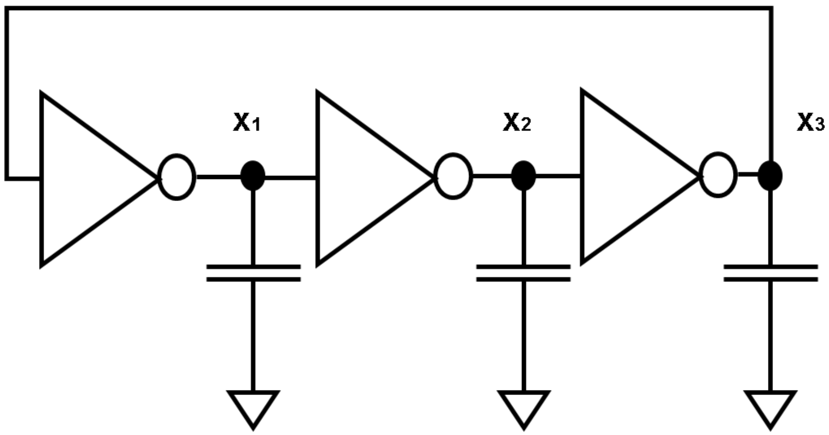
To which voltages will the nodes of the circuit settle if the inputs to the circuit remain indefinitely at their fixed values?

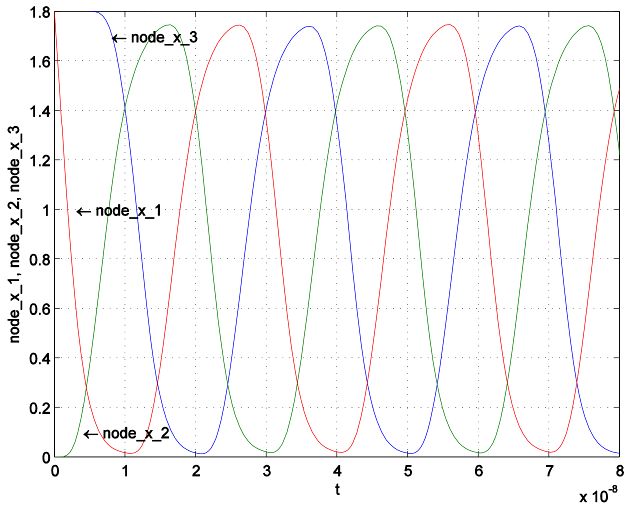
Some Applications

- Identify qualitative characteristics of a circuit (e.g., existence of stable behavior)
- Determine initial conditions prior to transient analysis
- Determine linearization point prior to ac small signal analysis

Ring Oscillators: A Motivating Example

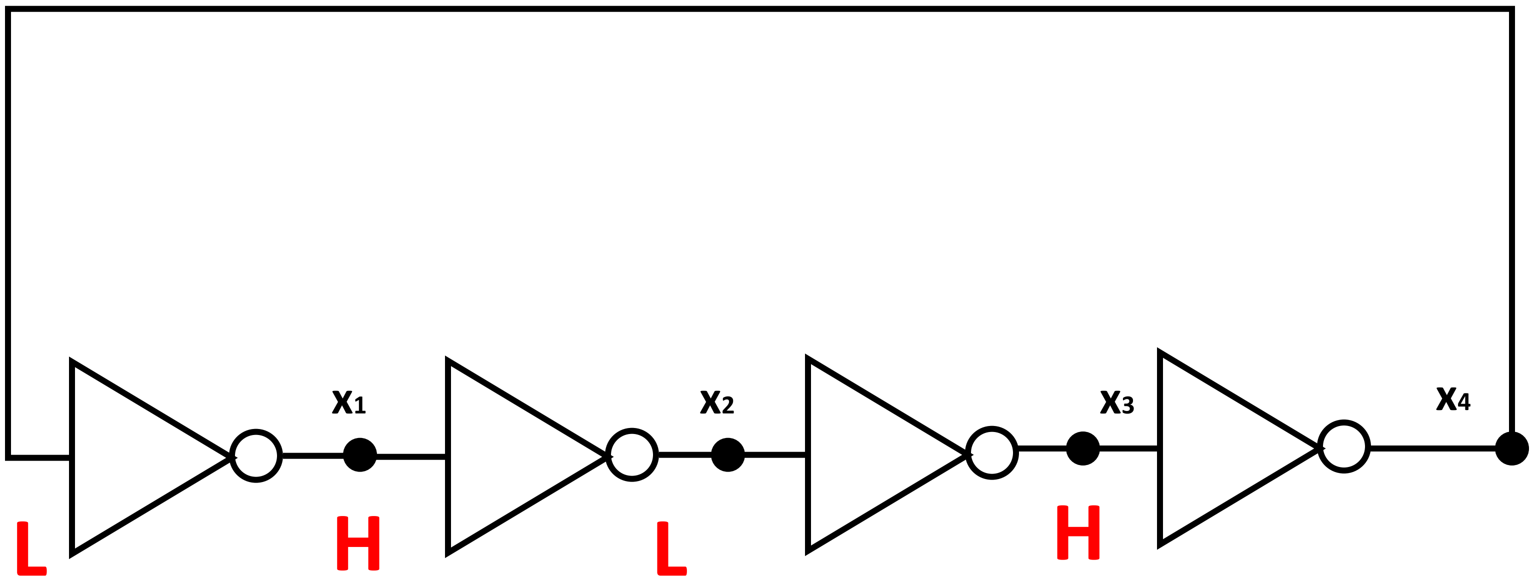
- Ring oscillators are a common component used in a variety of analog applications
- Uses an odd number of inverter stages to produce oscillating "0" and "1" signals



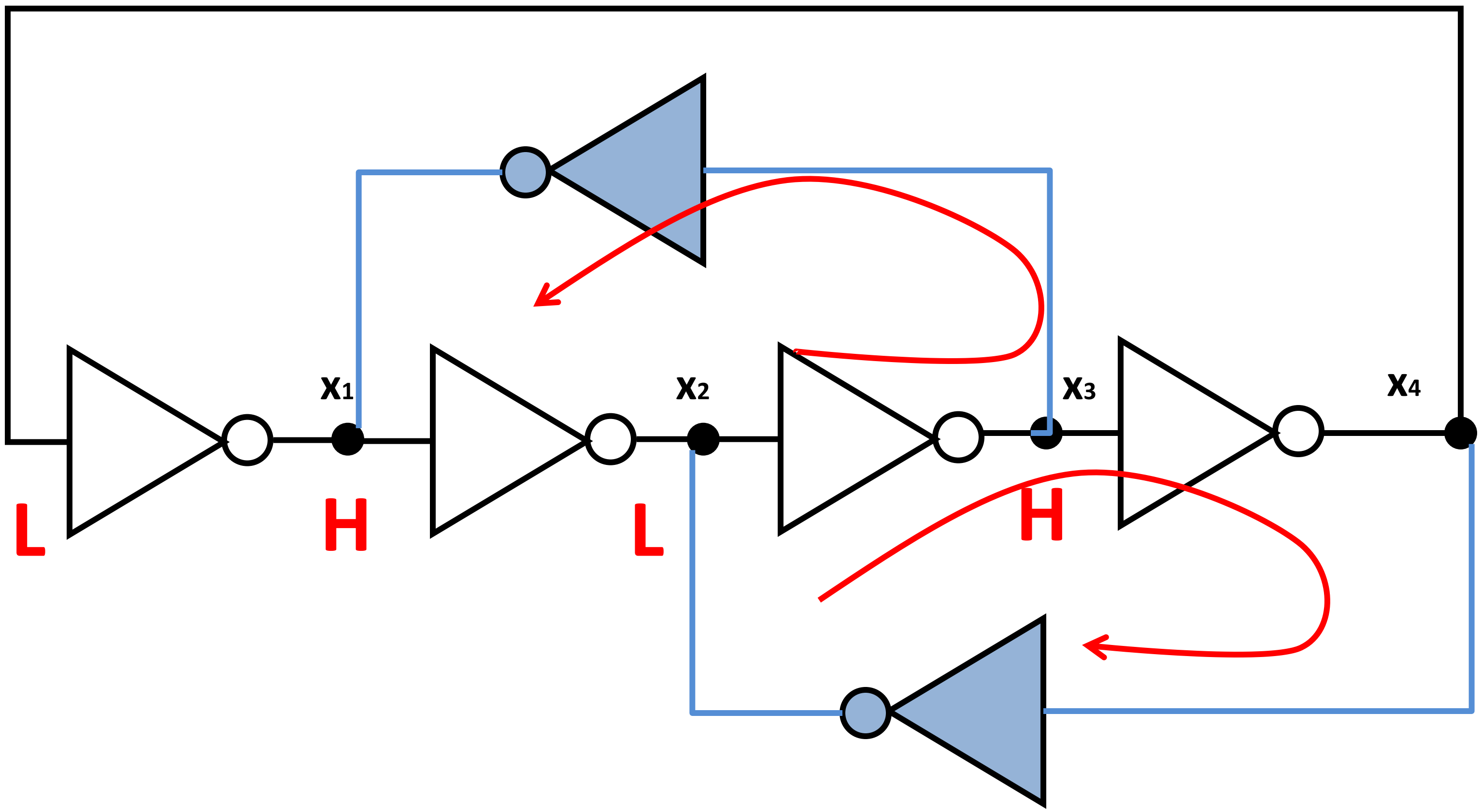


- Can we generate quadrature signals using ring oscillators?

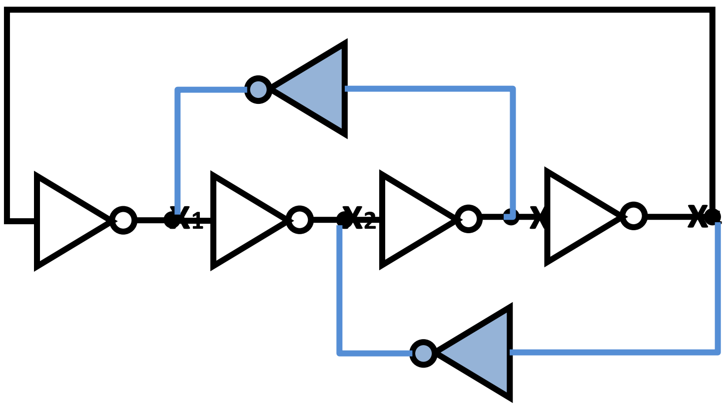
Rambus Oscillators

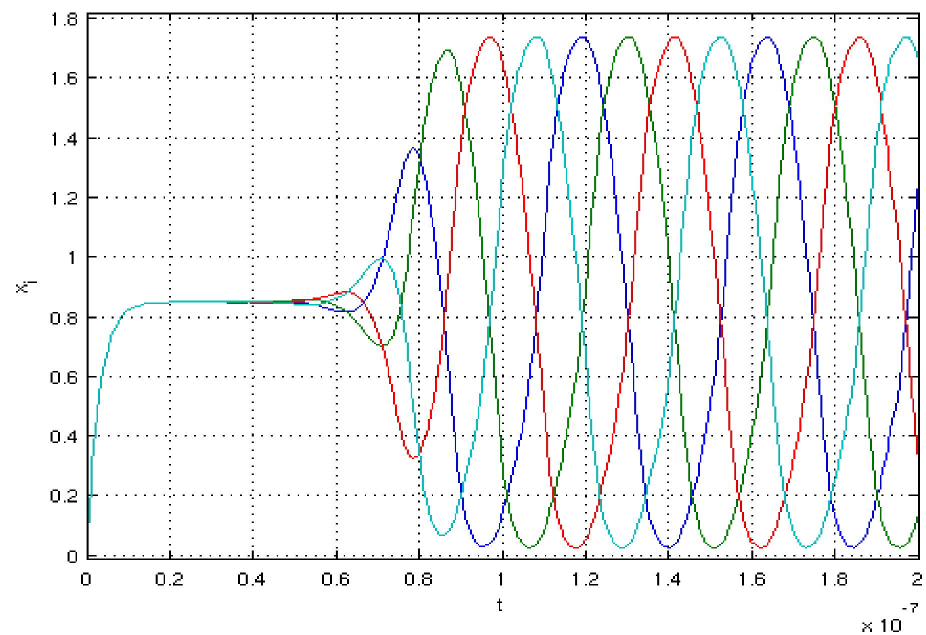


Rambus Oscillators



Rambus Oscillators



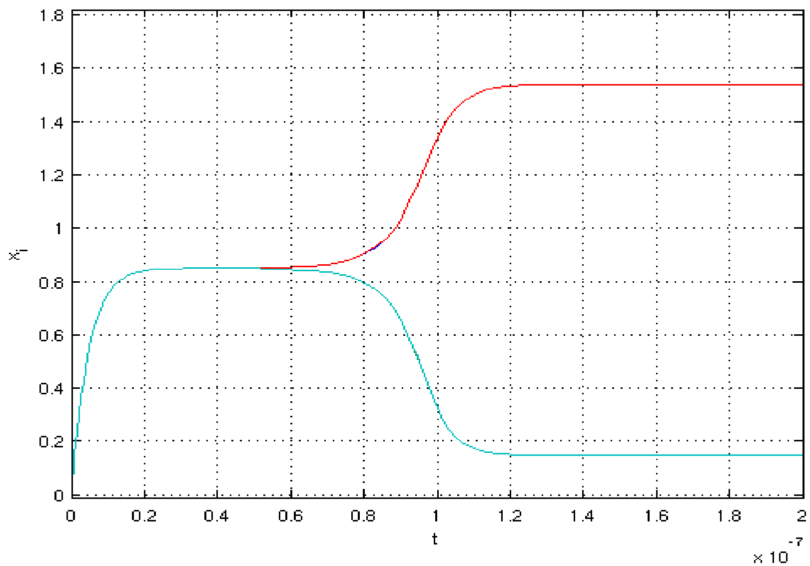


Circuits Parameters are guessed

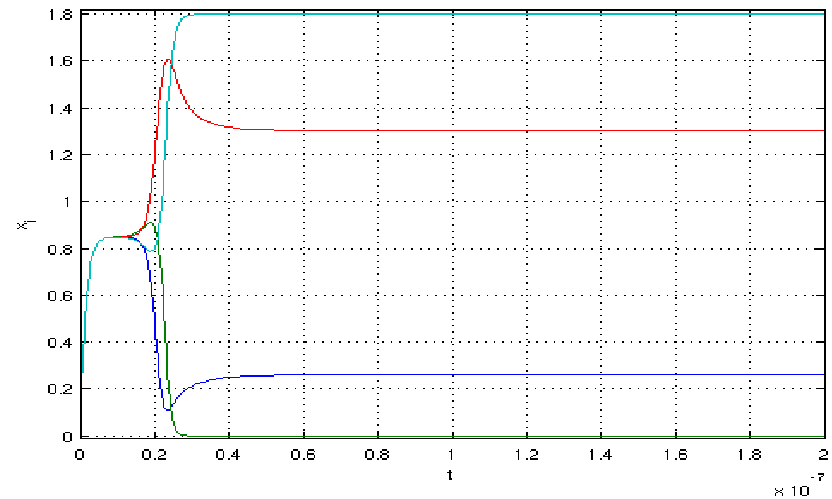
Rambus Oscillators

r: ring inverter *b: bridge inverter*

Width Ratio = Wr/Wb >>1



Width Ratio = Wr/Wb <<1



For some ratios, there are some initial conditions that lead to oscillation, while others lead to stable behavior. **GLSVLSI'08**

- Digital abstraction doesn't hold
- Functionality is sensitive to the exact sizing
- Sensitivities to initial conditions for some sizes

An Example from the "Real world"

- The example is extracted from an actual design failure
  - Some issues were only found in measurement of fabricated test chips
  - The design was validated as well as any analog designs are in practice today

Challenges for Verification

For a given choice of transistor sizes, show that the circuit operates properly for $^{\vee}$ all initial conditions

almost

Slide based on Kevin Jones talk at FMCAD'09, Portland, USA

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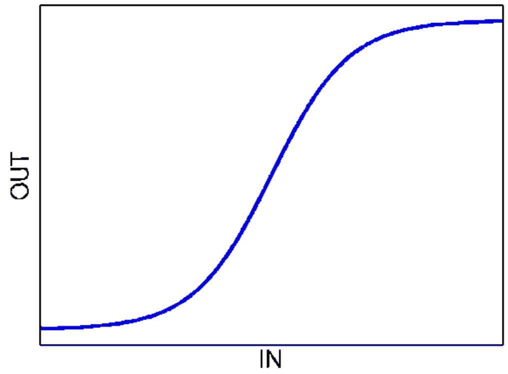
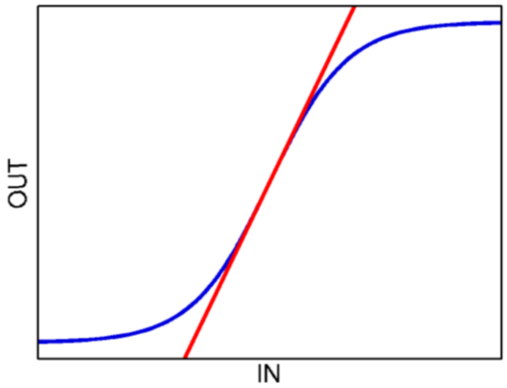
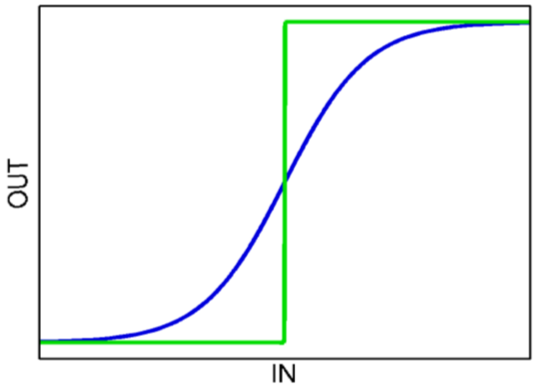
Circuits Modelling Views



Real world view



Analog world view



Digital world view

Slide based on Kevin Jones talk at FMCAD'09, Portland, USA

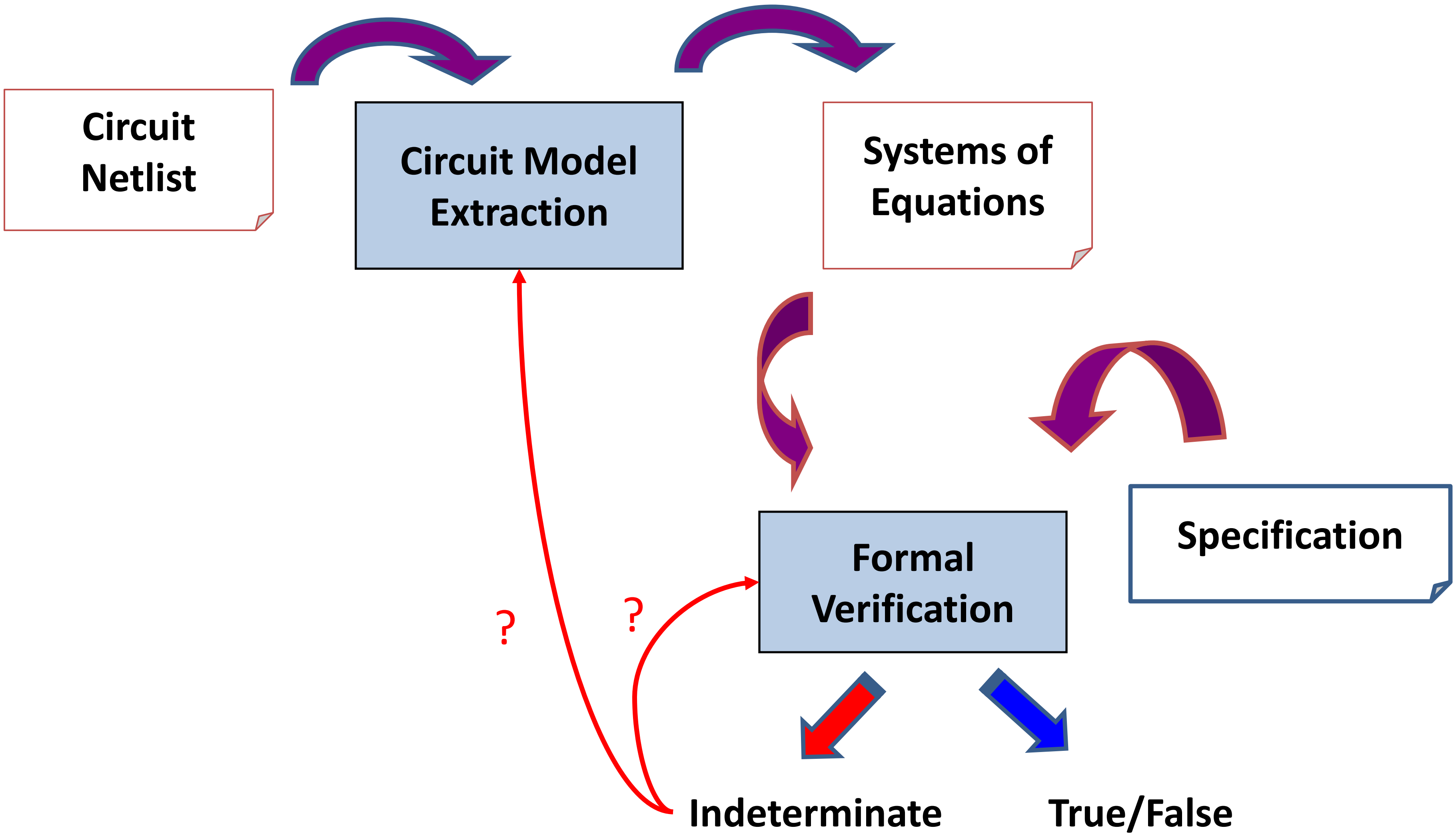
Challenges in Analog Verification

- Infinite continuous state space
  - Cannot do exhaustive simulation of individual traces/ trajectories
- Strong continuous nonlinear behavior
  - No closed form solution for differential equations
  - Numerical methods have inaccuracies
- Properties are hard to specify

Formal Verification

- Use mathematical reasoning to prove correctness
- Exploration of all the possible behaviors
- Assures implementation matches specification
  - If correct, all behaviors are verified
  - If incorrect a counter-example (proof) is presented
- Verification is undecidable
  - Indeterminate results

Research Framework



Formal Verification of Analog Circuits

Kurshan '91, Hartong'02,

- **State space decomposition, use numerical methods to build transitions**

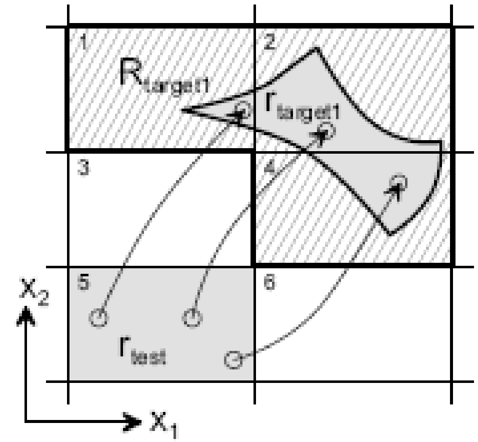
Greenstreet '98, 07, Gupta'04, Dang'04, Frehse'06, Little'04' 06

- **Forward Reachability: Geometrical enclosure of the behavior**

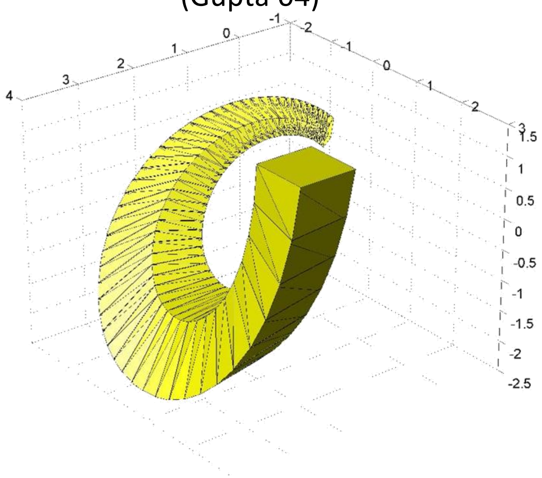
Freibothe'06, Walter'07, Tiwari'09, Denman'09

- **Constraints based Verification: Decision procedured (e.g., SMT) Linearization of the behavior**

(Kurshan'92)



(Gupta'04)



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DC Analysis

DC operating point: To which voltages will the nodes of the circuit settle to if the inputs to the circuit remain indefinitely at their fixed values?

Is it a requirement to have a DC operating point?

How many DC operating points does the circuit have?

Latch	Schmitt Trigger	Oscillator
2 DC OP	1 or 2 DC OP	0 DC OP

DC Equilibrium

Given an ODE system

$$\frac{d}{dt}x = f(x, in)$$

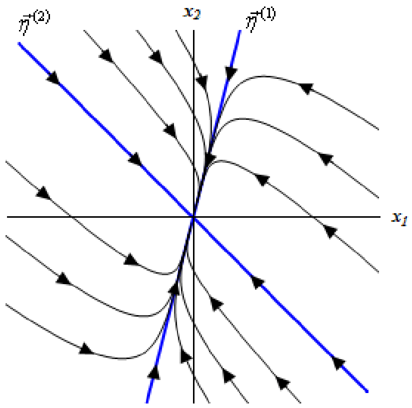
Necessary condition for existence of DC operating point

Chosen input

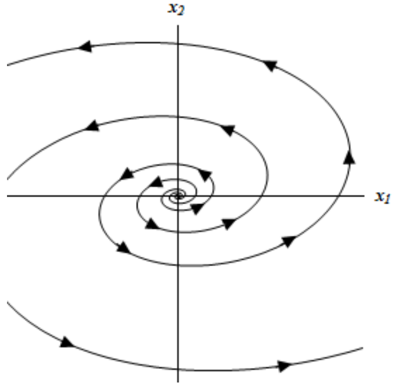
$$f(x, \underline{in}) = \mathbf{0}$$

What is the nature of the DC equilibrium points?

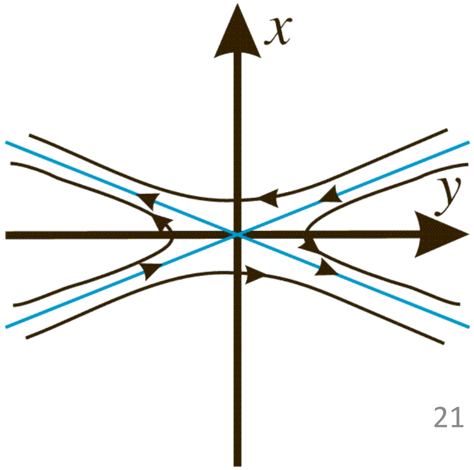
Stable Equilibrium: DC Operating point



Unstable Equilibrium



Metastable Equilibrium



Classifying DC equilibrium

Behavior of trajectories in the neighborhood of an equilibrium point is governed by the eigenvalues of the Jacobian matrix

J is Jacobian Matrix

Chosen input

$$J_{i,j}(f,\underline{x},\underline{in}) = \frac{\partial}{\partial x_j} f_i(x,\underline{in})\Big|_{x=\underline{x}}$$

- If all eigenvalues have real parts that are less than zero, then $\underline{x}$ *is a* *stable* *equilibrium* point ⟹ DC operating point

- If any eigenvalue has a positive real part, then we will call $\underline{x}$ *an* *unstable* *equilibrium* ⟹ *no DC operating point*

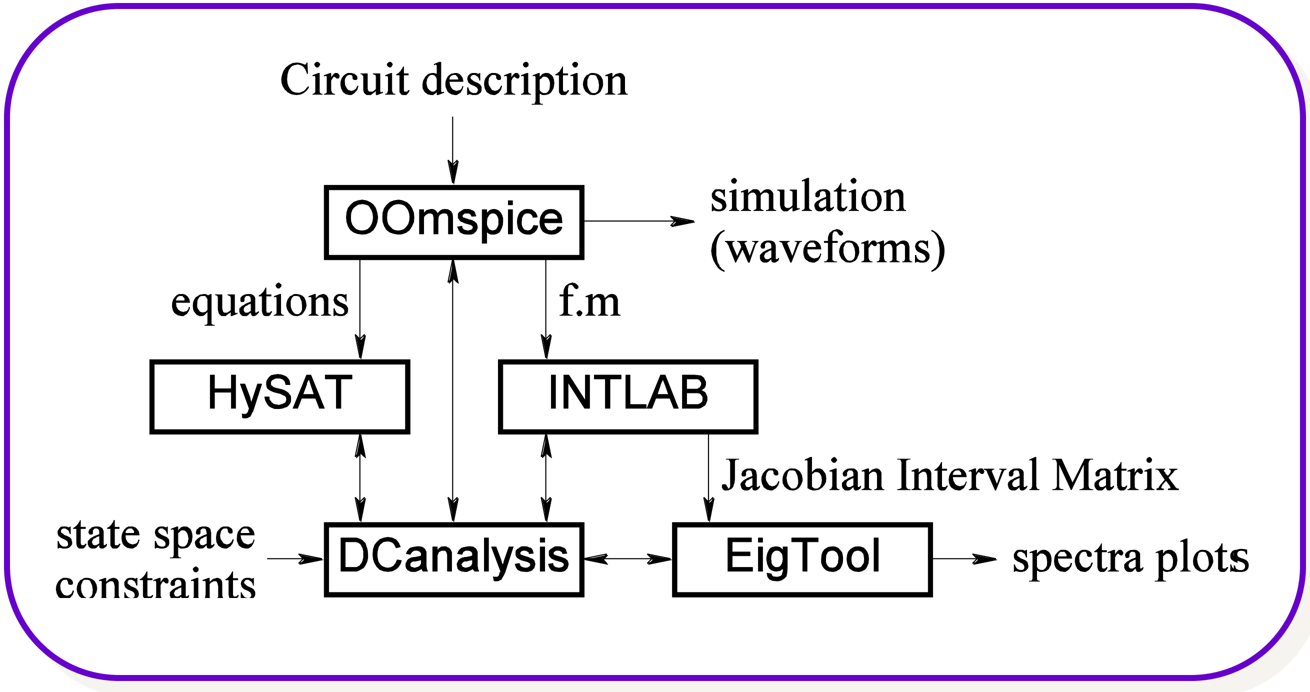
Issues in locating DC Operating points

- Finding a solution to the equations of a circuit involves finding the root of a system of non-linear equations

- Symbolic and numerical methods might fail to locate all possible solutions and be guaranteed to find a solution.

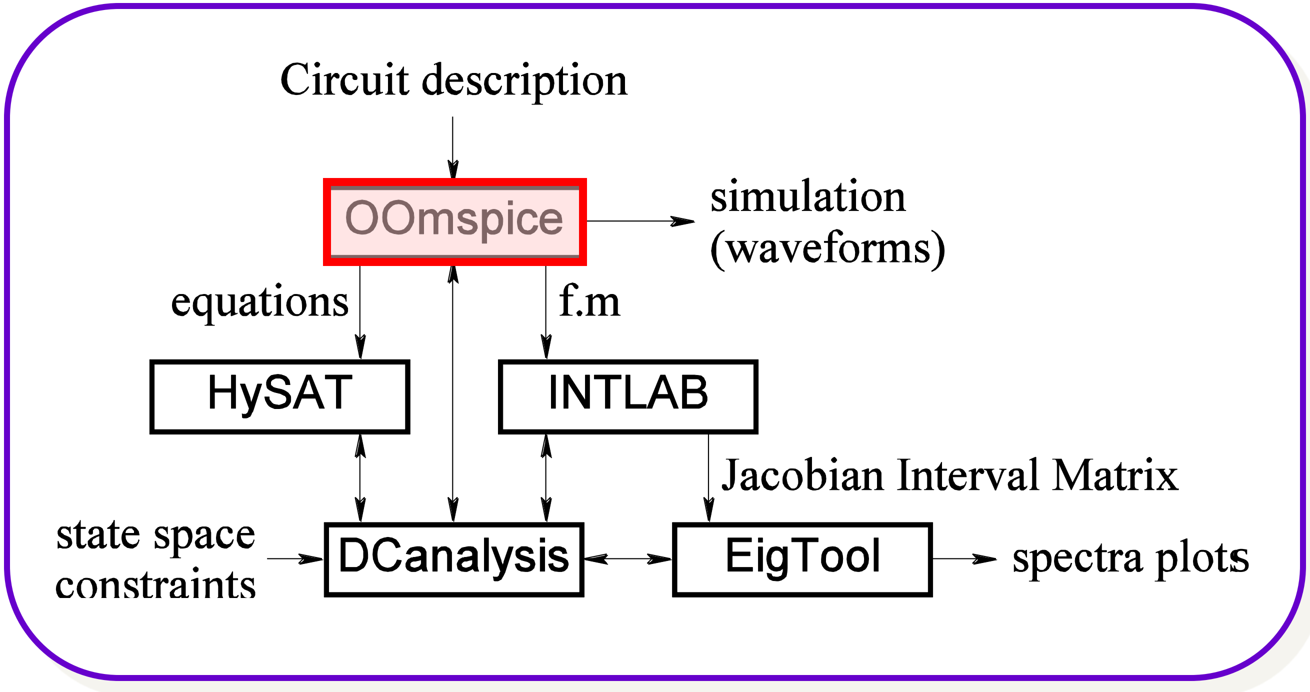
- If DC equilibriums are approximately identified, how to analyze their stability?

Proposed Approach



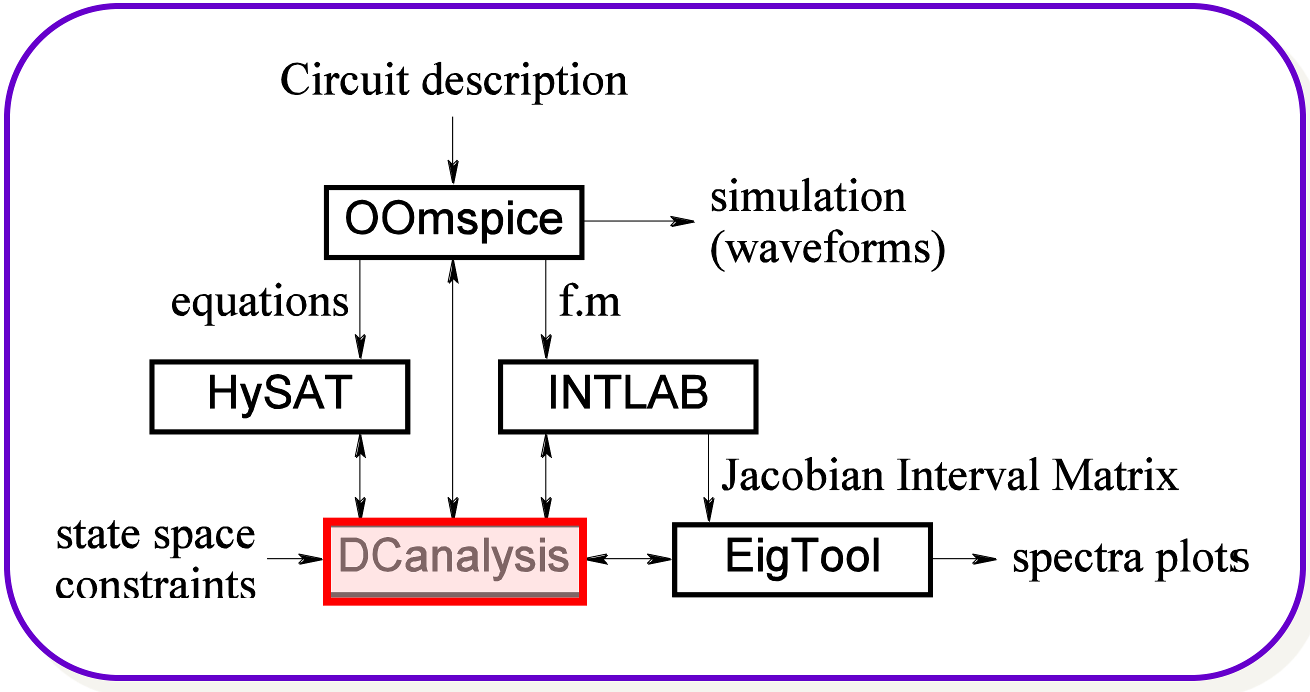
- Procedure that uses symbolic models generated from a netlist to rigorously locate and classify all of the equilibrium points
- Determines the existence, location and number of DC OP
- Implemented with a collection of public tools within MATLAB environment

Proposed Approach



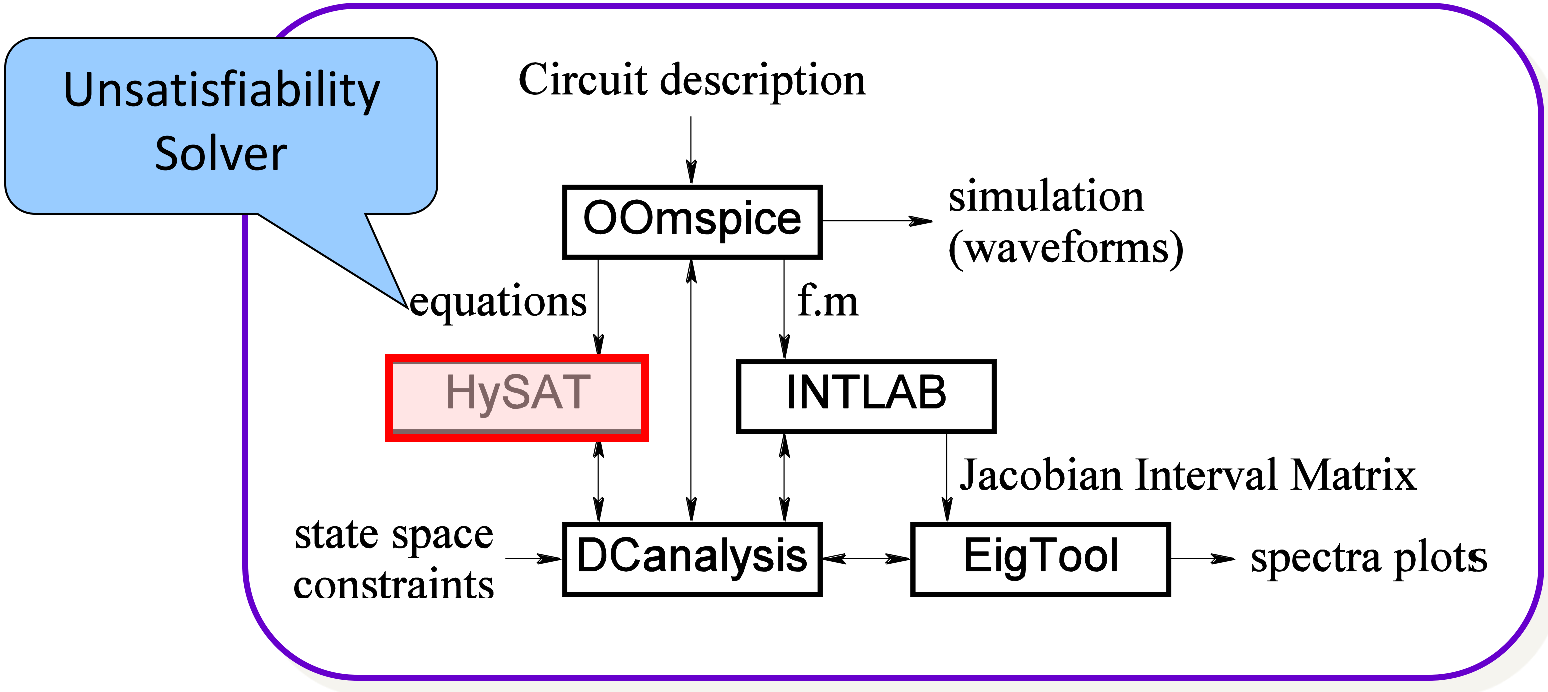
- **OOMSPICE:** **O**bject **O**riented **M**atlab **S**pice
- Circuit modeling and analysis for formal verification
- Accommodates the creation of hierarchical designs
- Possible addition of new electrical components and alternative abstractions descriptions of existing components.

Proposed Approach



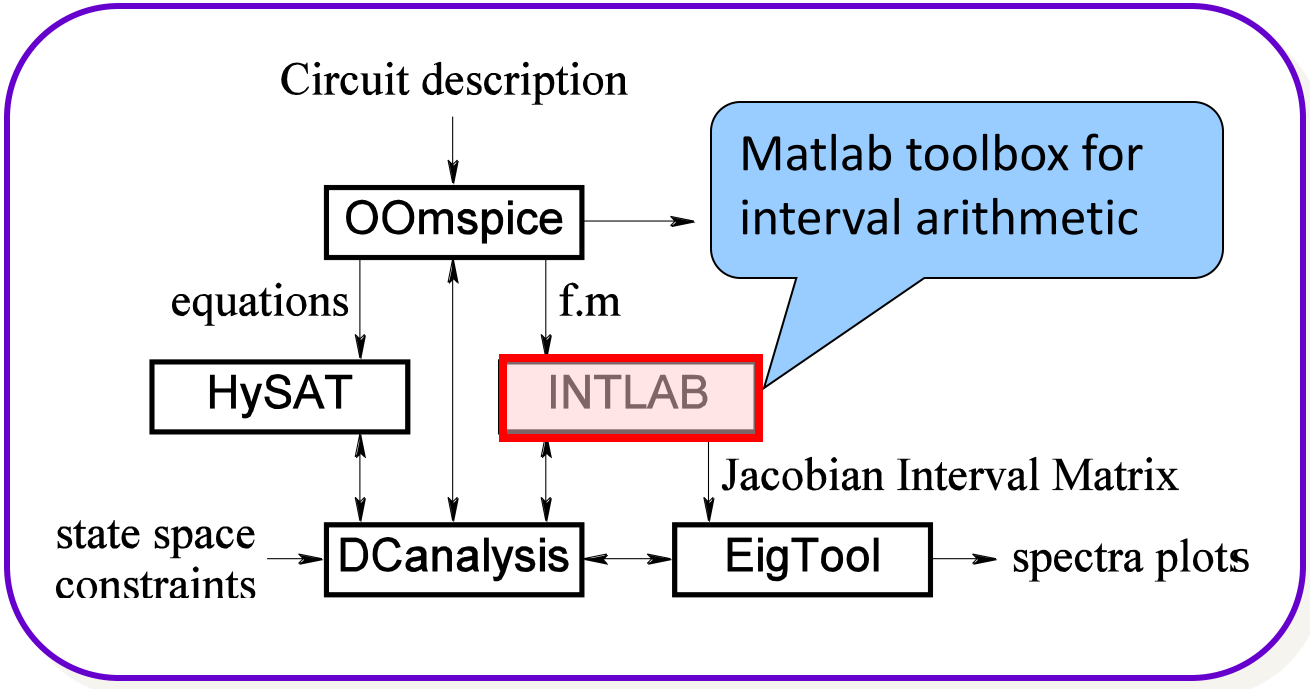
- Coordinates the verification tasks and uses OOmspice to generate the circuit equations as desired by the verification tools:
- DC equations for Hysat
- ODE system for INTLAB

Proposed Approach



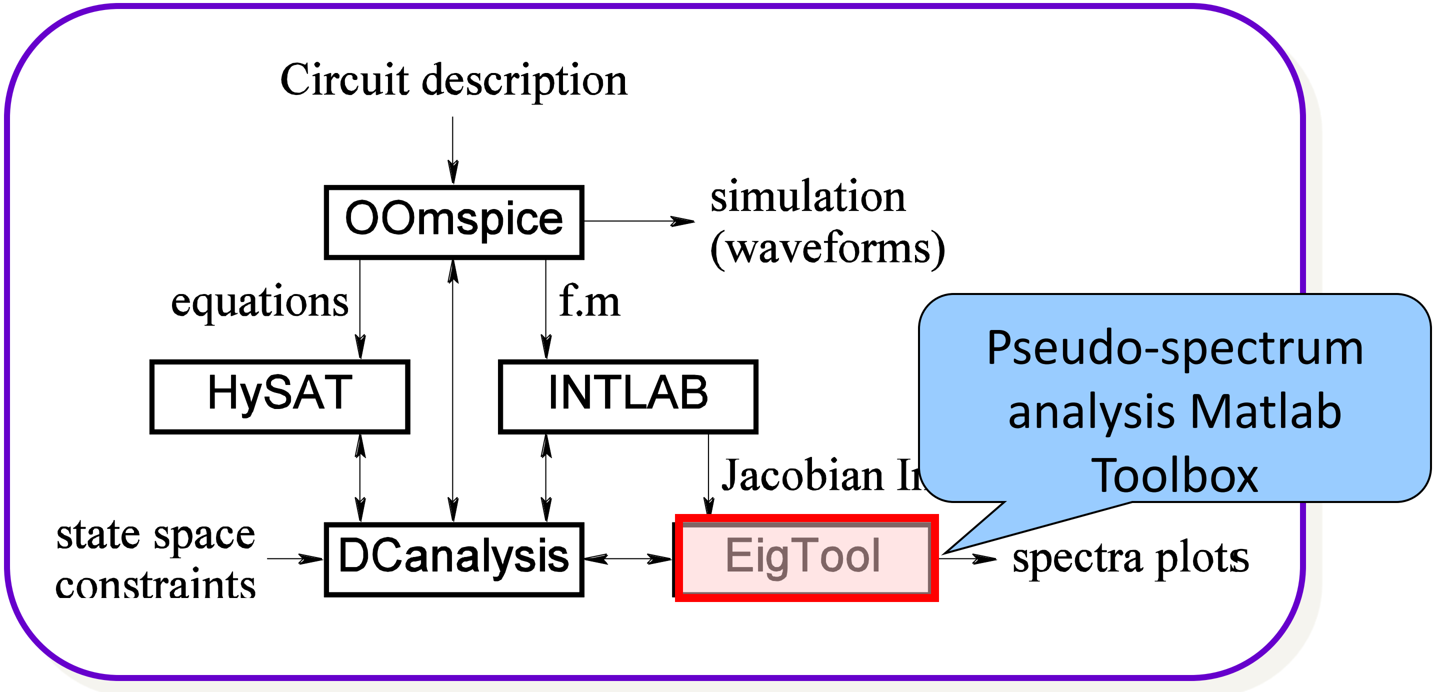
- HySAT identifies regions Q that might contain DC equilibria
- Iterative calls until HySAT establishes that the remaining space does not contain any equilibria
- Candidate regions Q forwarded to INTLAB for further analysis

Proposed Approach



- Refutes regions with no DC equilibriums
- Provides tighter bounds for regions which includes equilibrium points
- Provides Jacobian Interval matrices for all points in a given region

Proposed Approach

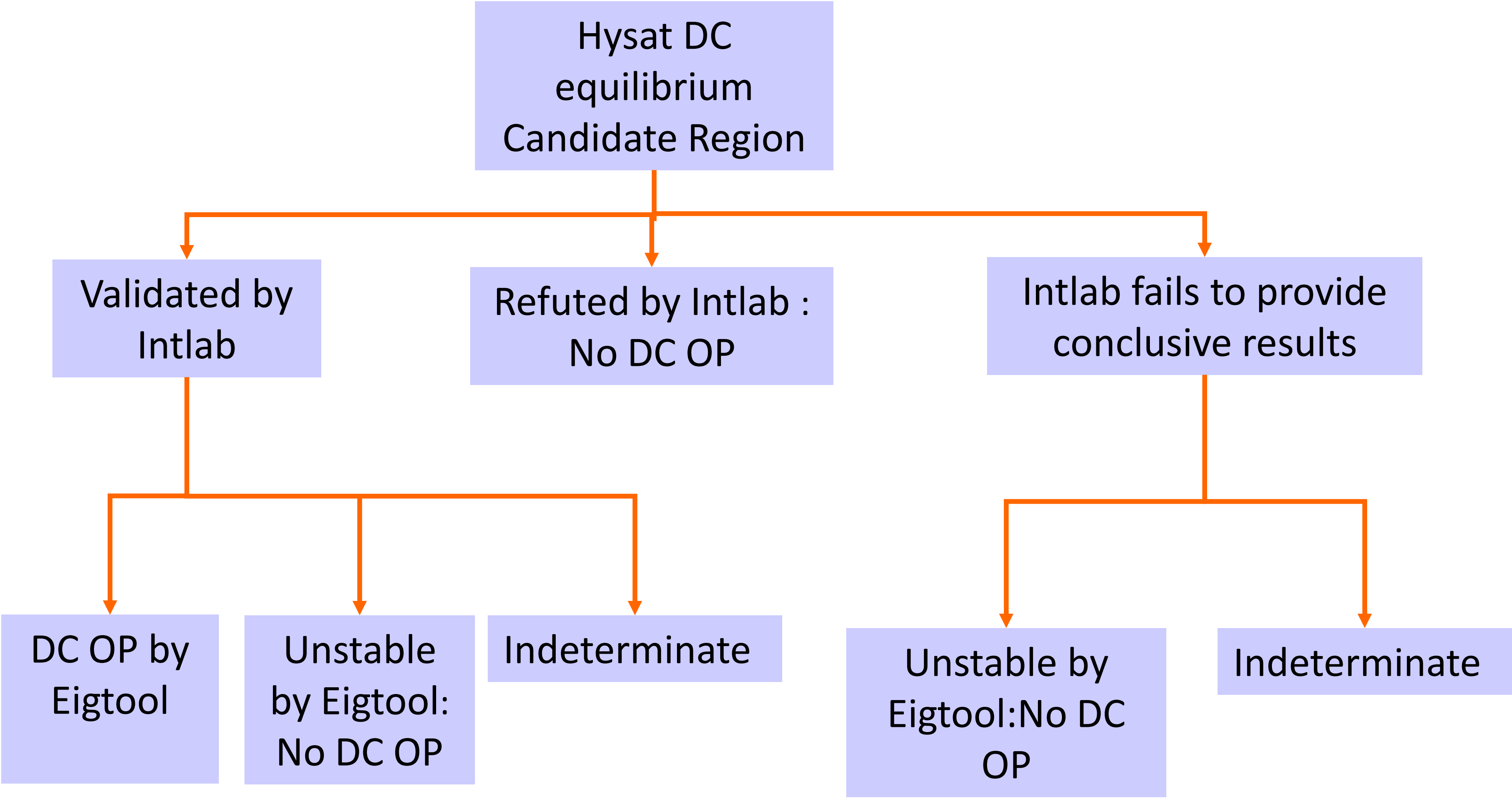


- We seek to categorize the stability of any equilibrium as definitely stable, definitely unstable, and unknown.

- Region does not contain a DC operating point if all matrices in provided Interval Matrix have at least one eigenvalue with positive real component

- Region contains a DC operating point if all matrices in provided Interval Matrix have all eigenvalues with negative real component

Verification Outcome



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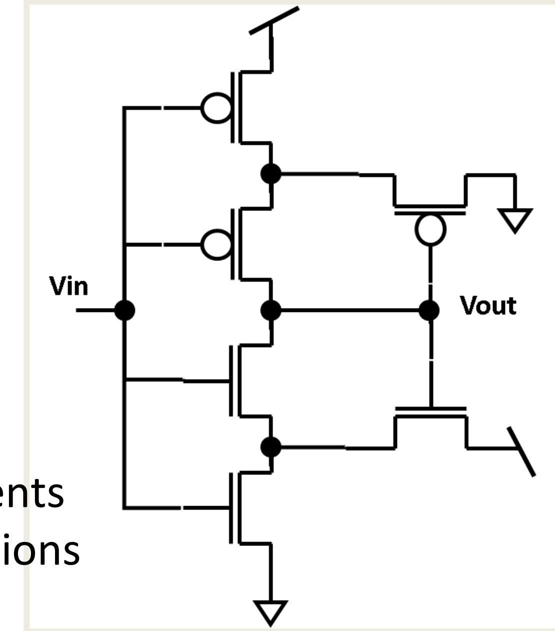
Schmitt Trigger




```matlab
function  m = Schmitt_Trigger

%Parameters for First Order Transistors model
trn_params = 'Trans_params';
% Gate, Source and Drain Capacitance
C = [0.55e-15, 0.55e-15/2, 0.55e-15/2];
% Input Signal parameters
Pulse_params = 'pulse_param';

Vin1 = Voltage_Source_Pulse('Vin1', Pulse_params);
Vdd = Supply_Voltage('Vdd', 1.8);
Gnd = Ground('Gnd', 0);
NMos1 = NmosCell('NMos1', trn_params, C);
PMos1 = PmosCell('PMos1', trn_params, C);
PC = Trans_series('PC', trn_params, C, -1);
NC = Trans_series('NC', trn_params, C, 1);

m = connect_pins(m, Vdd, NMos1.D, 'node_vdd');
m = connect_pins(m, Vdd, PC.Vs);
m = connect_pins(m, Gnd, PMos1.D, 'node_gnd');
m = connect_pins(m, PC.Vgnd, Gnd);
m = connect_pins(m, NC.Vgnd, Gnd);
m = connect_pins(m, Gnd, Vin1.N);
m = connect_pins(m, Gnd, NC.Vs);
m = connect_pins(m, PC.Out, PMos1.S, 'node_y1');
m = connect_pins(m, NC.Out, NMos1.S, 'node_y2');
m = connect_pins(m, Vin1.P, PC.In, 'node_in');
m = connect_pins(m, Vin1.P, NC.In);
m = connect_pins(m, PMos1.G, PC.Vd, 'node_out');
m = connect_pins(m, NMos1.G, PC.Vd);
m = connect_pins(m, PC.Vd, NC.Vd);

m = end_circuit(m);
```

Parameters

Components Instantiations

Pins Connections

Schmitt Trigger Cicruit Equations

```
function dydt = Schmitt_Trigger_model(t,y)

Cap_node_out_V_Port = y(1,:);
Cap_node_y2_V_Port = y(2,:);
Cap_node_y1_V_Port = y(3,:);

Vin1_V_Port = fun_pulse(t,'pulse_params')';
node_gnd_V = 0;
node_vdd_V = 1.80;
node_in_V = node_gnd_V+Vin1_V_Port;
node_y2_V = node_gnd_V+Cap_node_y2_V_Port;
node_y1_V = node_gnd_V+Cap_node_y1_V_Port;
node_out_V = node_gnd_V+Cap_node_out_V_Port;
Pmos1_PC_Ids = fun_mos(node_in_V,node_vdd_V,node_y1_V,-1,'Trans_Params');
Nmos1_NC_Ids = fun_mos(node_in_V,node_gnd_V,node_y2_V,1,'Trans_Params');
Nmos2_NC_Ids = fun_mos(node_in_V,node_y2_V,node_out_V,1,'Trans_Params');
Pmos2_PC_Ids = fun_mos(node_in_V,node_y1_V,node_out_V,-1,'Trans_Params');
PMos1_Ids = fun_mos(node_out_V,node_y1_V,node_gnd_V,-1,'Trans_Params');
NMos1_Ids = fun_mos(node_out_V,node_y2_V,node_vdd_V,1,'Trans_Params');
Cap_node_out_I_Port = -Pmos2_PC_Ids-Nmos2_NC_Ids;
Cap_node_y2_I_Port = -Nmos1_NC_Ids+Nmos2_NC_Ids+NMos1_Ids;
Cap_node_y1_I_Port = -Pmos1_PC_Ids+Pmos2_PC_Ids+PMos1_Ids;

dydt = [Cap_node_out_I_Port/1.650000e-15;...
        Cap_node_y2_I_Port/8.250000e-16;...
        Cap_node_y1_I_Port/8.250000e-16];
```

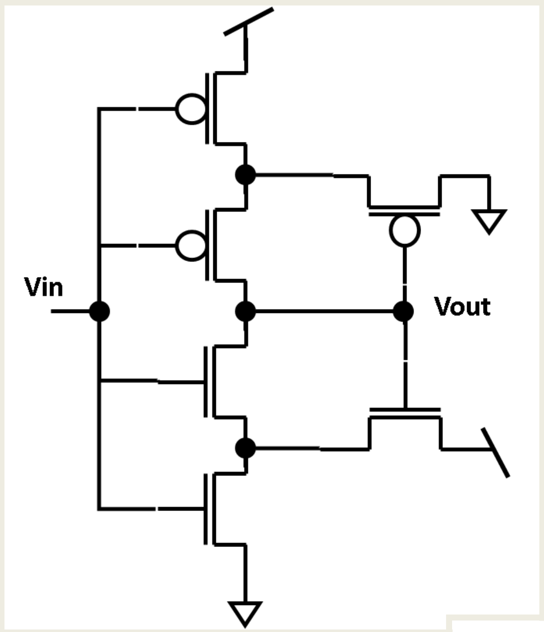
State Space

Equations

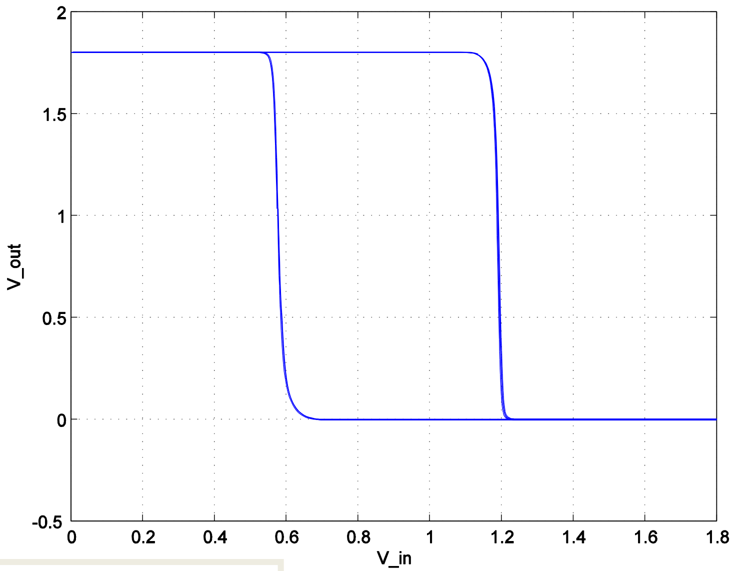
KCL

ODEs

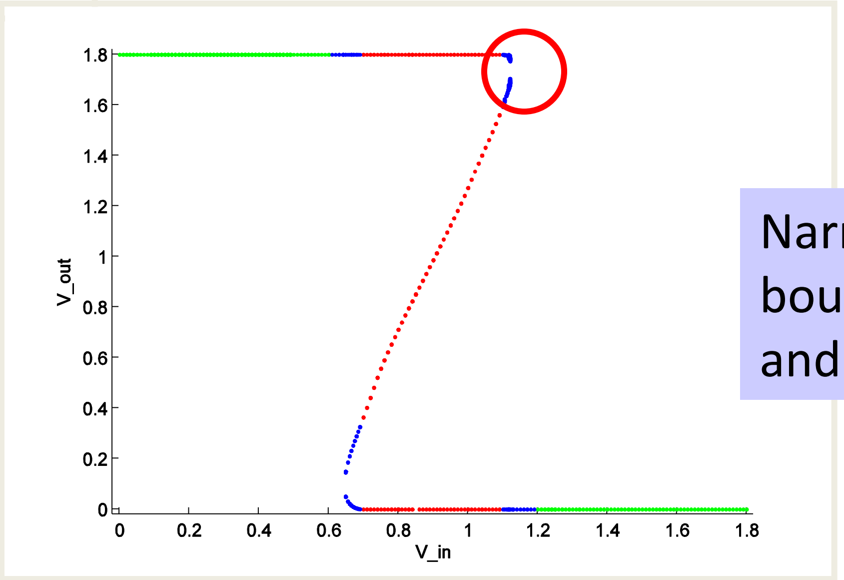
Schmitt Trigger



Schematic



Hysteresis



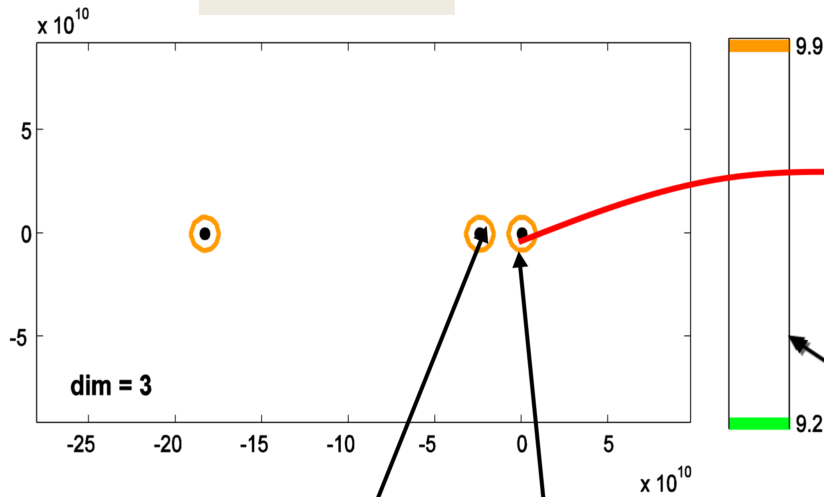
Narrow inconclusive bounds width of 0.007 and 0.006 in [0, 1.8]

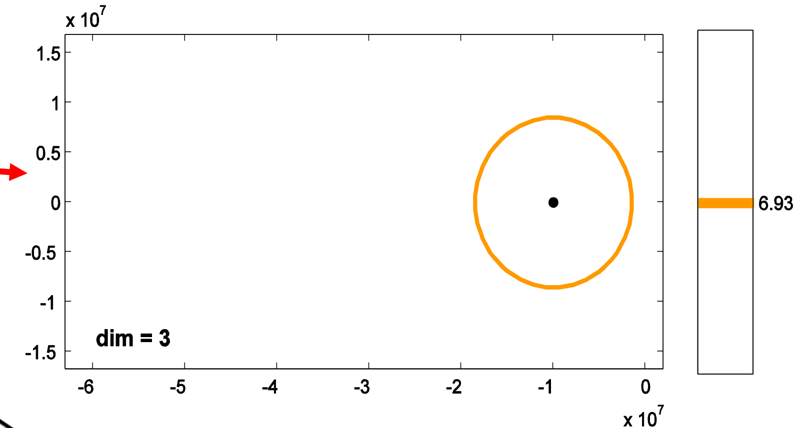
DC transfer Function

Schmitt Trigger

DC Operating Points

Vin = 1.8 V

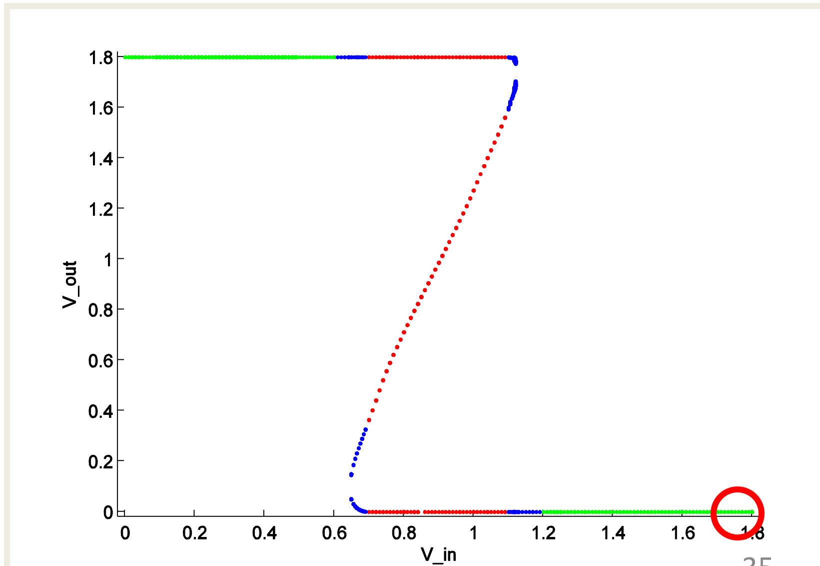




Norm of Offset Matrix (log scale)

Bounds on eigenvalue

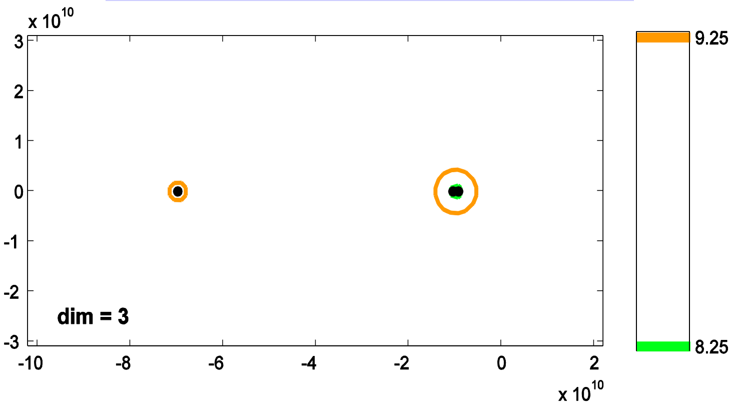
Eigenvalue of central matrix



Jacobian Interval Matrix = Central Matrix +/- Offset Matrix

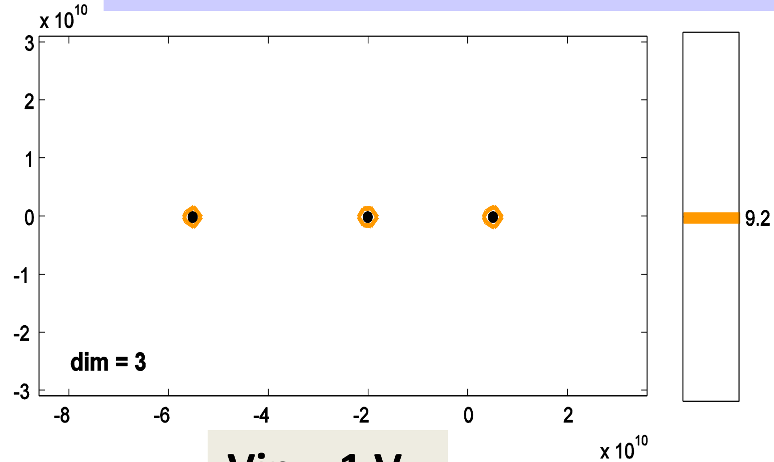
Schmitt Trigger

DC Operating Points



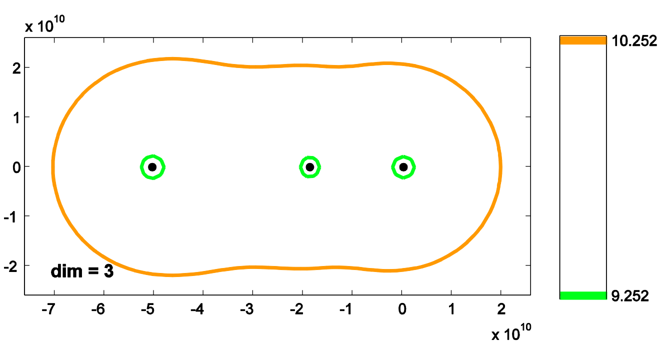
Vin = 0 V

Unstable Equilibria: Not DC OP

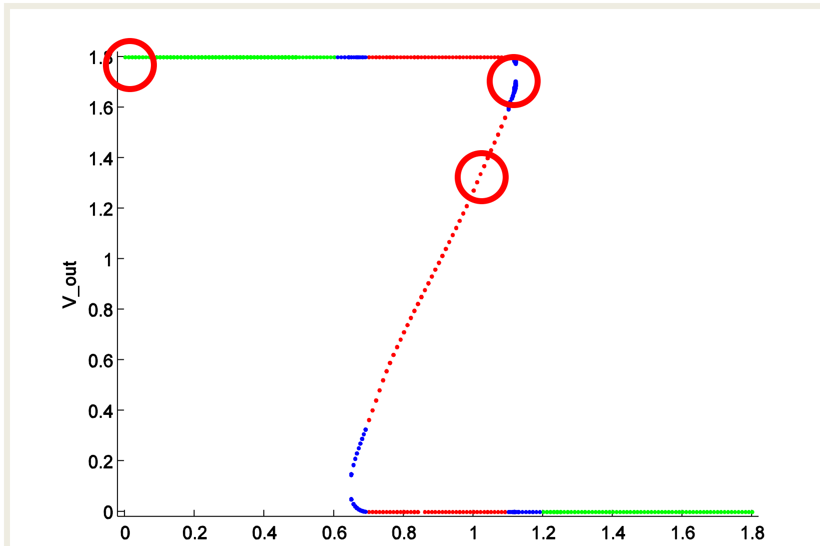


Vin = 1 V

Indeterminate case



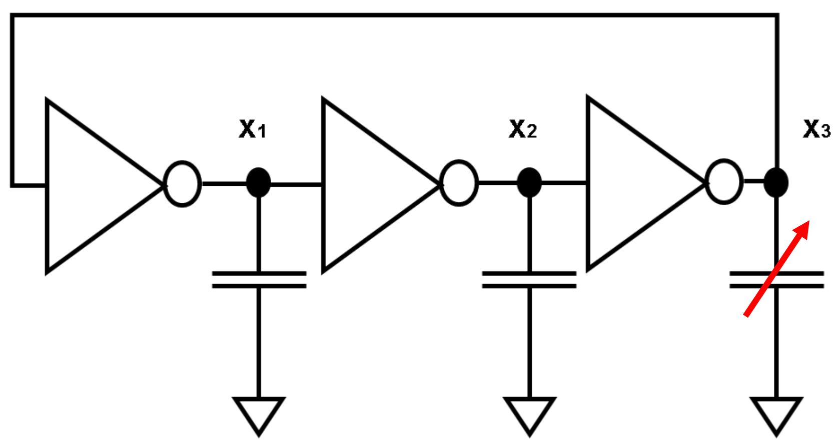
Vin = 1.124 V



Other Experimental Results:

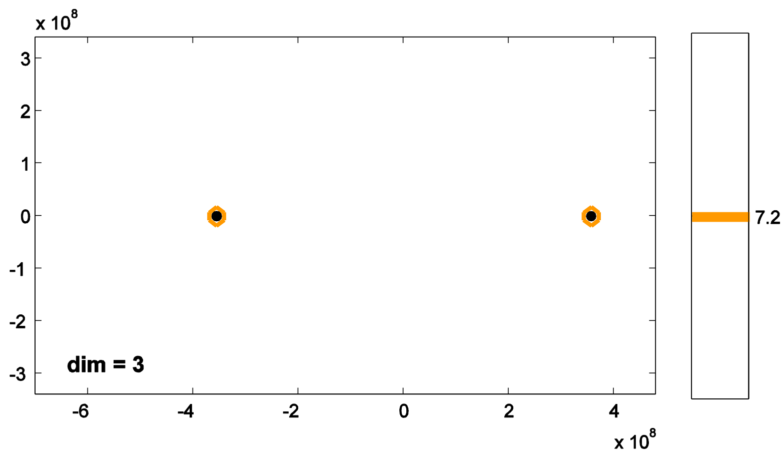
- Proved that Ring Oscillators with odd number of stages (up to 25 stages) do not posses DC operating points

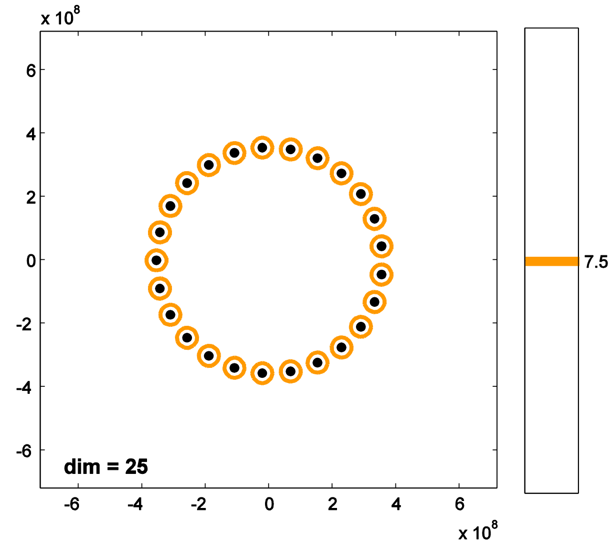
- Effect of load capacitance on the oscillation. Sufficient large capacitance load can break the oscillation



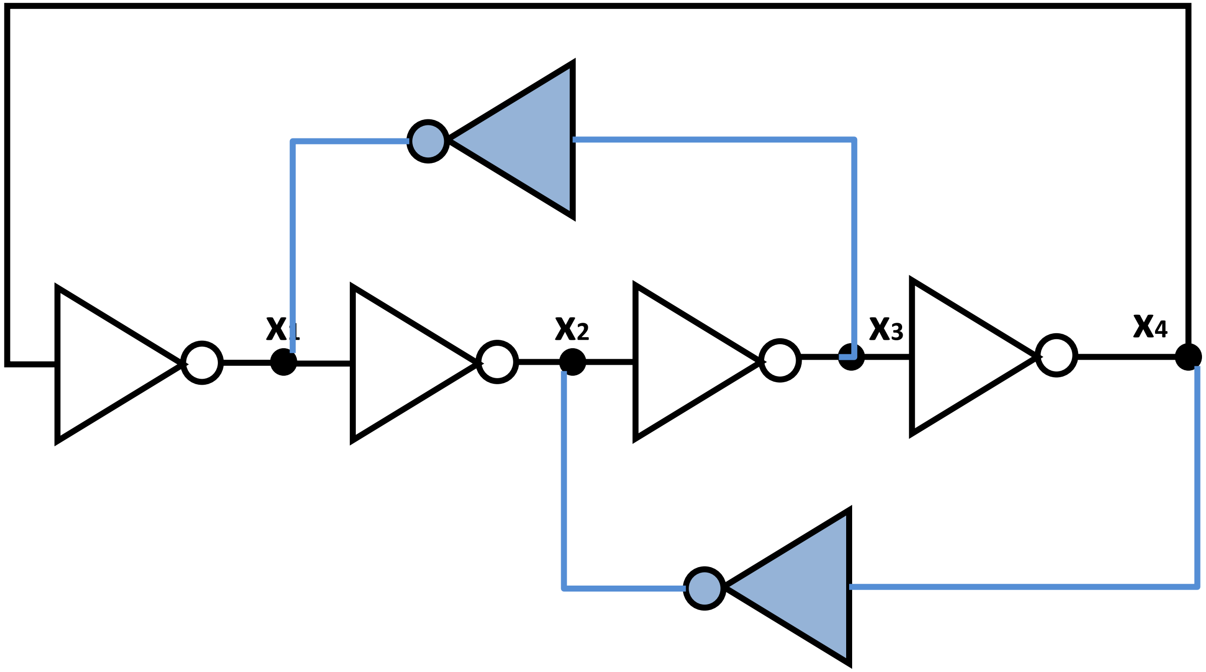
- Proved that Even number of Ring oscillators (up to 24 stages) always have stable state

Ring Oscillator: 3 and 25 stages





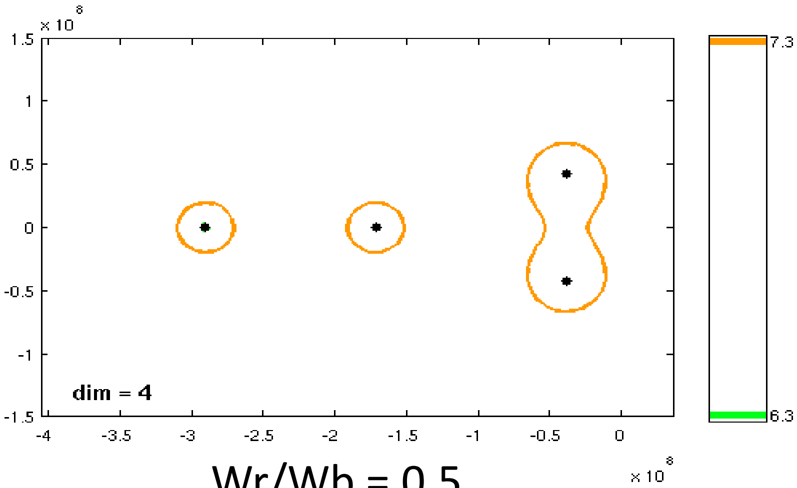
Rambus Oscillators



For a given choice of transistor sizes, show that the circuit operates properly for "almost all" initial conditions

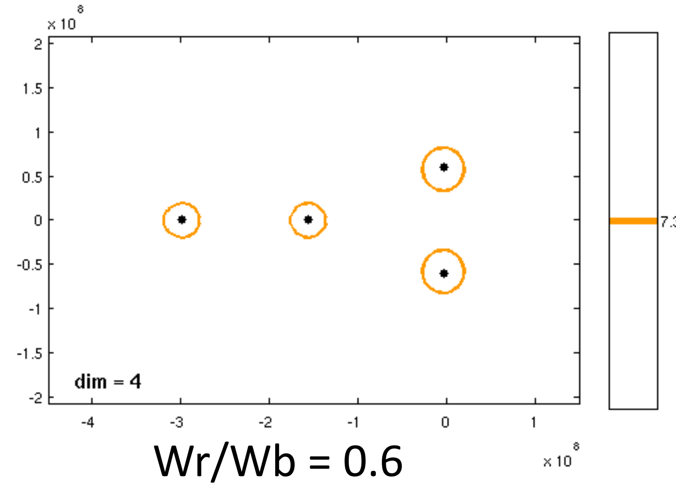
Rambus Oscillators

DC Operating Points



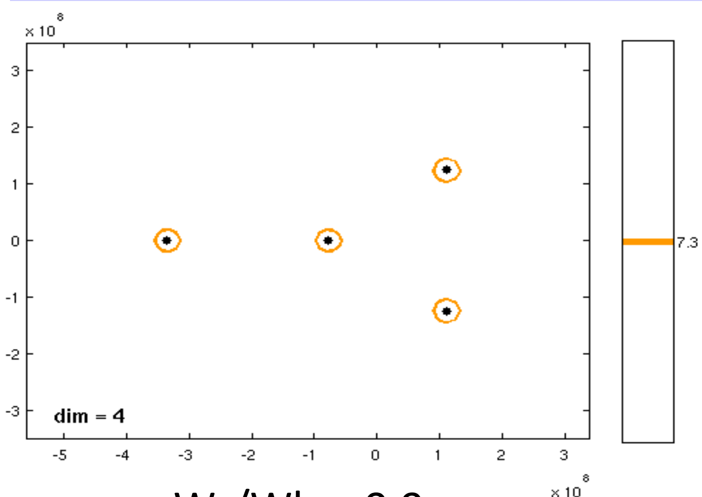
Wr/Wb = 0.5

Indeterminate



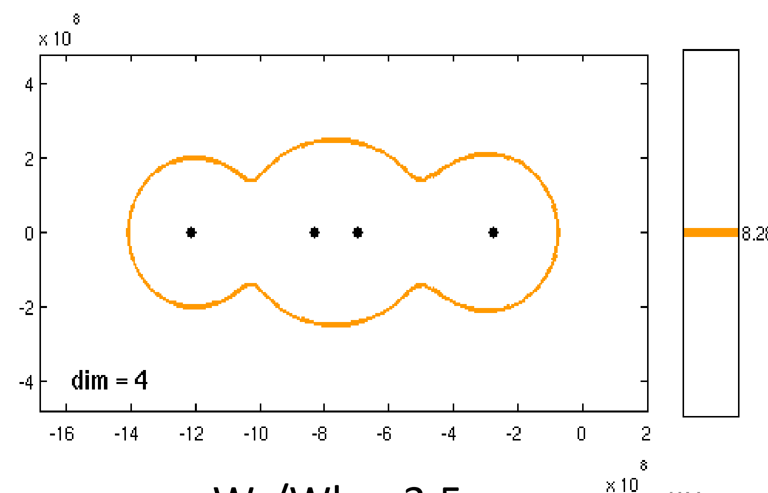
Wr/Wb = 0.6

Unstable Equilibria : Not DC OP



Wr/Wb = 0.9

DC Operating Points



Wr/Wb = 3.5

Talk Outline

- ❑ Introduction
- ❑ Formal Verification of Circuits: An Overview
- ❑ DC Analysis:
  - ❑ Basic Concepts
  - ❑ A Formal Approach
- ❑ Case Studies
- ❑ Enhancing the Verification with invariants
- ❑ Discussion

Invariant Checking

- Find upper and lower bounds on the operating state space.
- Given a constraint, is it a bound on the state space?
- For each state variable x:

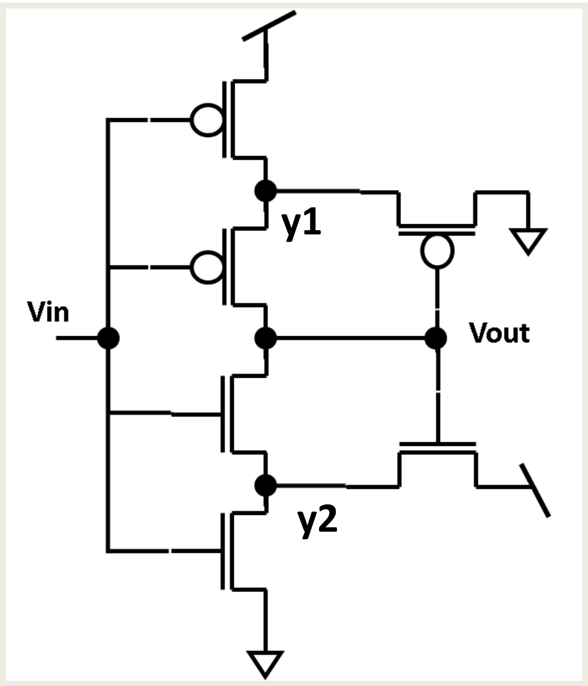
find b1 and b2 such that:

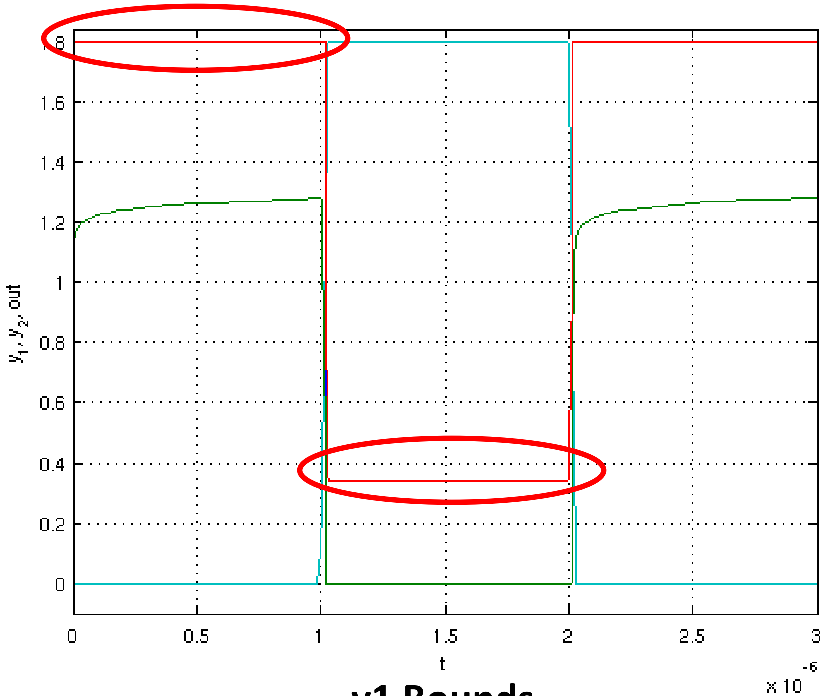
$$x = b2 \text{ implies } \dot{x} =< 0$$

and

$$x = b1 \text{ implies } \dot{x} >= 0$$

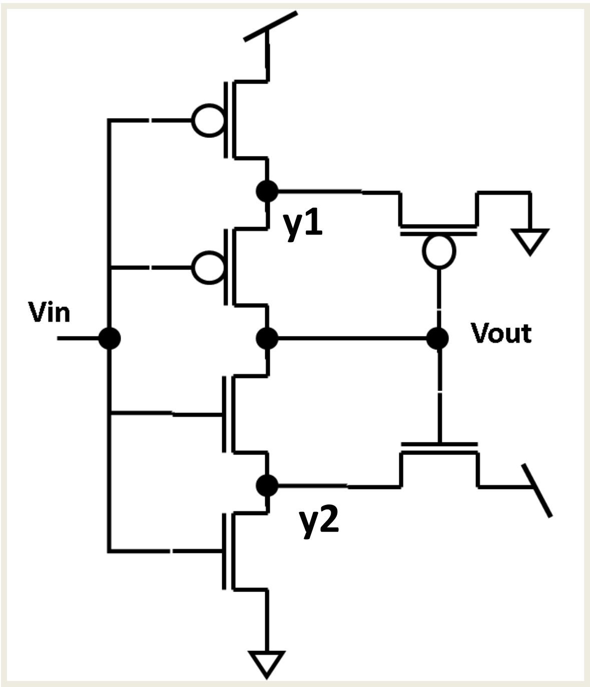
Invariant Checking: Schmitt Trigger

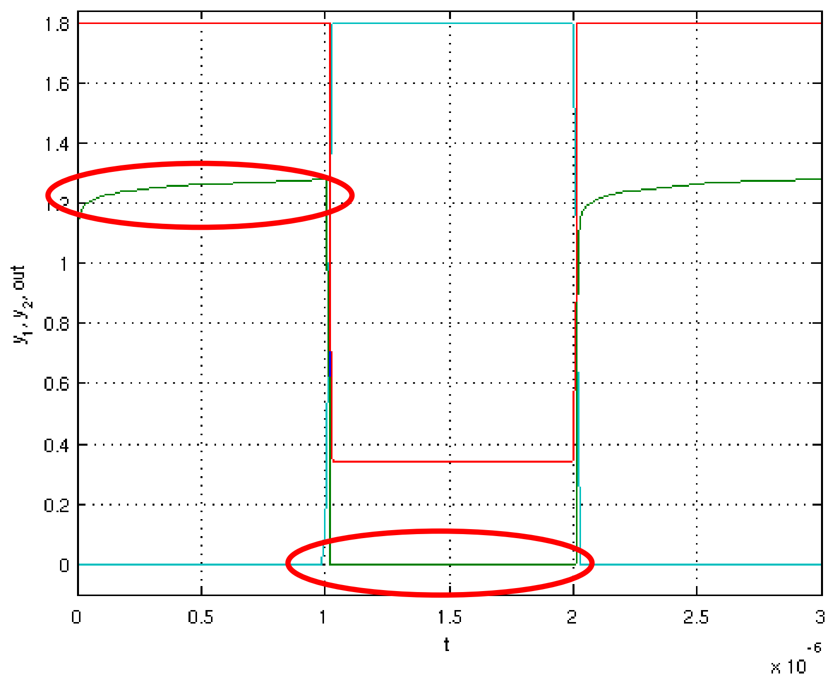




y1 Bounds

Invariant Checking: Schmitt Trigger

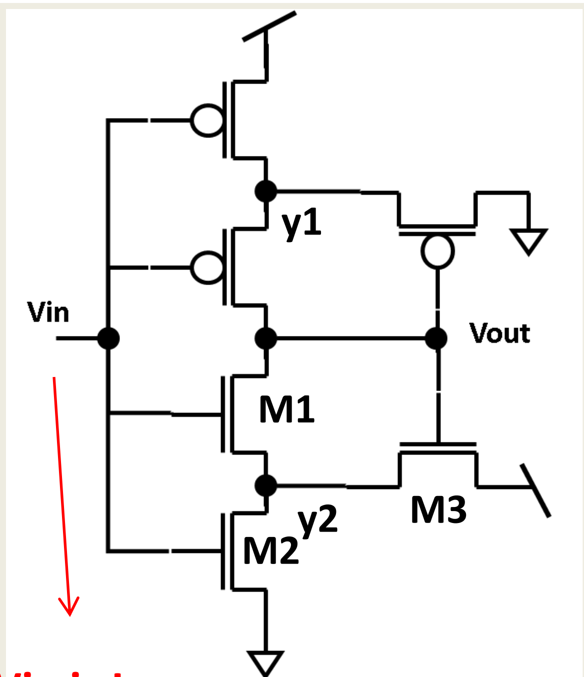


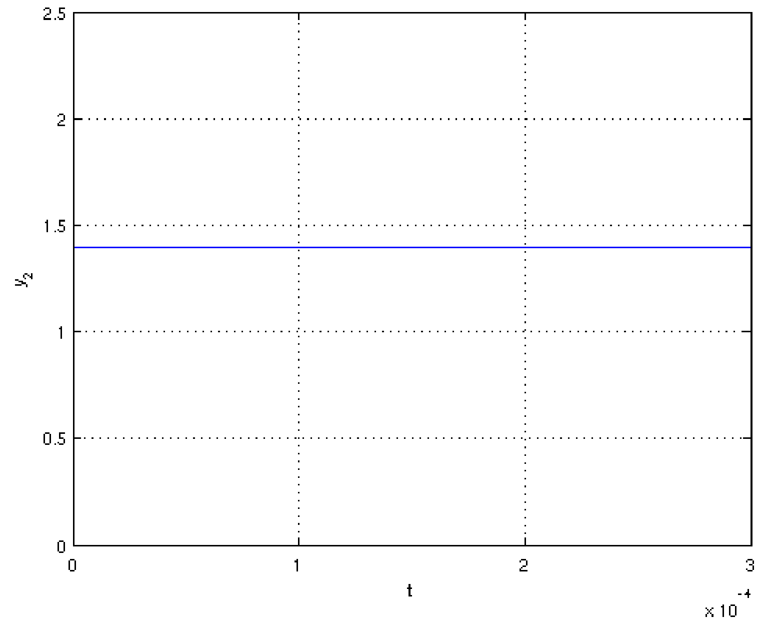


y2 Bounds

Invariant Checking: Schmitt Trigger

Problems with First Order Model





Vin is Low

➡ **M1 and M2 are off**

Suppose Initial V_y2 > b2

➡ **M3: Vgs < vth and M3 is off**

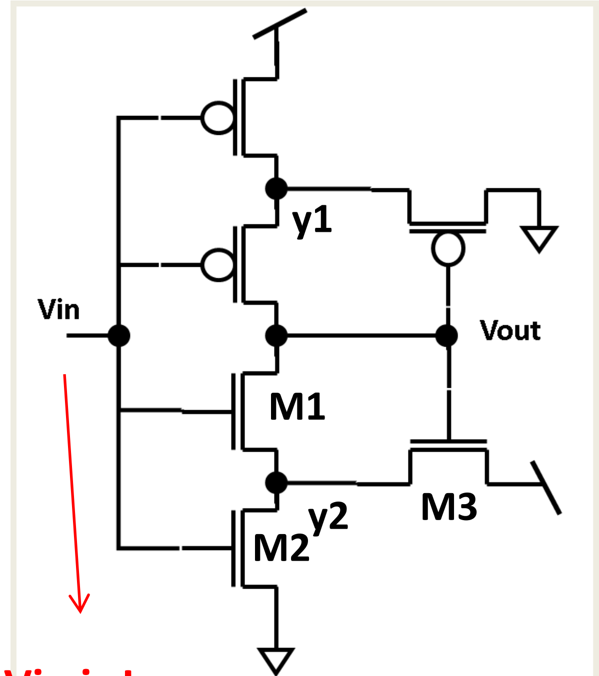
- **First order model does not consider subthreshold current (no leakage)**
- **Failure to prove bounds on voltage nodes for some input voltages**

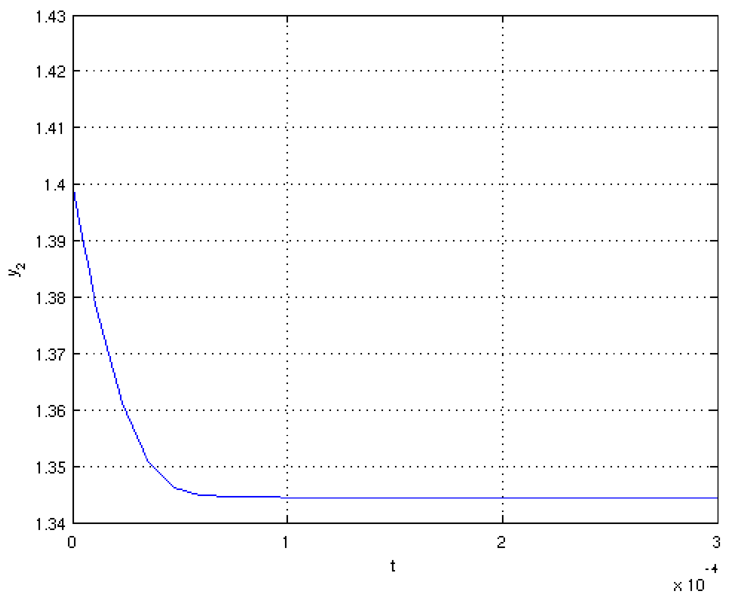
EKV Mosfet Model

- MOS model that provides a similar behavioral representation compared to spice models
- EKV Model is accurate even when the MOSFET is operating in the subthreshold region
- Closed form expressions that are continuous across the transistor operating regions.
- Hysat friendly

Invariant Checking: Schmitt Trigger

EKV Model





Vin is Low

→ **M1 and M2 are off**

Suppose Initial V_y2 > b2

→ **M2: Vgs < vth and M2 is off**

- **EKV mode considers subthreshold current (no leakage)**
- **Bounds were proved automatically**

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Challenges Outlined in FMACD'08 Talk on Open Analog Problems

- Avoiding transient simulation
- Establishing that operating point assumptions are valid
- Establishing that all initial conditions result in correct behavior
- Dealing with non-linearity

Conclusion

- Tackling DC analysis in a more formalized way
- Identifying and classifying DC operating points of circuits using a collection of tools in the open domain
- Demonstrating the presented methodology on a variety of circuits

Is formal verification possible for Analog Designs?

Formal methods is possible. But is it effective??

Primary Results say YES

I've got this pain in all the diodes down my left side*.

* From the Hitchhiker's Guide to the Galaxy, by Douglas Adams